10/719,218

Corr

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Wang et al.

Attorney Docket No.:
ALTRP100/A1198

Patent No.: 7,427,813 B1

Issued: September 23, 2008

Title: STRUCTURE, MATERIAL, AND DESIGN FOR ASSEMBLING A LOW-K SI DIE TO ACHIEVE AN INDUSTRIAL GRADE RELIABILITY WIRE BONDING PACKAGE

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on October 28, 2008 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Quyen Vuong

## REQUEST FOR CERTIFICATE OF CORRECTION (35 U.S.C §255, 37 C.F.R. §1.323)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing.

Several mistakes of a clerical or typographical nature, or minor in character appears in the above-referenced patent; however, the mistake occurred in good faith. The correction introduces no new matter nor requires reexamination. The mistake occurred because of a typographical error.

The errors together with the exact page and line number where the errors appear in the application file are as follows:

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01 FC:1811 100.00 OP

Certificate
NOV 04 2008
of Correction

NOV - 4 2008

**CLAIMS:**

1. In line 16 of claim 1 (column 11, line 33) change "active" to --top--. This error appears in the Amendment F as filed on January 29, 2008, on page 2 line 14.

2. In line 2 of claim 4 (column 11, line 47) change "other" to --of the--. This appears correctly in the Amendment F as filed on January 29, 2008, on page 2, line 25.

3. In line 2 of claim 11 (column 12, line 19) change "front" to --from--. This appears correctly in the Amendment F as filed on January 29, 2008, on page 3, line 17.

Check No. 2362 in the amount of $100.00 is enclosed in accordance with 37 CFR § 1.20(a). However, if it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 504480
(Order No. ALTRP100/A1198).

Respectfully submitted,
Weaver Austin Villeneuve & Sampson LLP

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NOV - 4 2008

PTO/SB/44 (10-96)
Approved for use through 6/30/99. OMB 0651-0033
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE


(Also Form PT-1050)

# UNITED STATES PATENT AND TRADEMARK OFFICE
# CERTIFICATE OF CORRECTION

PATENT NO. : 7,427,813 B1

DATED : September 23, 2008



INVENTOR(S) : Wang et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**CLAIMS:**

1. In line 16 of claim 1 (column 11, line 33) change "active" to --top--.

2. In line 2 of claim 4 (column 11, line 47) change "other" to --of the--.

3. In line 2 of claim 11 (column 12, line 19) change "front" to --from--.

MAILING ADDRESS OF SENDER:

PATENT NO. 7,427,813 B1

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# PROOFED

**To:** **Cindy H. Shu**

**From:** **Quyen Vuong**

**Date:** **October 22, 2008**

**Docket:** **ALTRP100**

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**CLAIMS:**

1. In line 16 of claim 1 (column 11, line 33) change "active" to --top--. This error appears in the Amendment F as filed on January 29, 2008, on page 2 line 14.

2. In line 2 of claim 4 (column 11, line 47) change "other" to --of the--. This appears correctly in the Amendment F as filed on January 29, 2008, on page 2, line 25.

3. In line 2 of claim 11 (column 12, line 19) change "front" to --from--. This appears correctly in the Amendment F as filed on January 29, 2008, on page 3, line 17.


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5. (Previously Presented): A semiconductor package as recited in claim 4, wherein the molding interface material is also on a corresponding adjacent portion of the packaging substrate in order to secure the die to the packaging substrate.

6. (Currently Amended): A semiconductor package as recited in claim 1, wherein the molding interface material is applied in multiple non-contiguous regions to the **[[active]]** **top** surface of the die.

7. (Original): A semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is rectangular in shape.

8. (Original): A semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is triangular in shape.

9. (Original): A semiconductor package as recited in claim 6, wherein each of the multiple non-contiguous regions has a thickness of less than 2 microns.

10. (Currently Amended): A semiconductor package as recited in claim 1, wherein the molding interface material is a contiguous region on the **[[active]]** **top** surface of the die excluding corner regions.

11. (Original): A semiconductor package as recited in claim 10, wherein the contiguous region is offset from the corner regions by about 100 to 150 microns.

12. (Currently Amended): A semiconductor package as recited in claim 10, wherein the molding interface material is a contiguous region on the **[[active]]** **top** surface of the die excluding edge regions.

13. (Original): A semiconductor package as recited in claim 12, wherein the contiguous region is offset from the edge regions by about 100 to 150 microns.

14. (Original): A semiconductor package as recited in claim 1, wherein the molding interface material has a coefficient of thermal expansion between 5 ppm and 40 ppm.

The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended): A semiconductor package comprising:

a die having a plurality of layers of low-K dielectric material in the die, the die having a **[[active]]** **top** surface including circuitry fabricated thereon, a non-active surface **not including circuitry**, and a plurality of side surfaces, each surface having associated corner and edge regions;

a wire bonding packaging substrate having a plurality of electrical contacts, the packaging substrate being positioned under the die;

a plurality of interconnects electrically connecting the die to the plurality of electrical contacts;

a molding interface material applied to at least a portion of the **[[active]]** **top** surface of the die, the molding interface material being configured to control at least one of tensile and shear stresses experienced by the die in the proximity of the active surface; and

a molding cap **including a molding compound** covering at least a portion of the die, packaging substrate, interconnects, and the molding interface material;

**wherein the molding interface material is a discrete layer separate from the molding compound and formed between the molding cap and the die**.

2. (Previously Presented): A semiconductor package as recited in claim 1, wherein the molding interface material is configured to introduce compressive stress to the die and strengthen the die against the at least one of tensile and shear stresses.

3. (Previously Presented): A semiconductor package as recited in claim 1, wherein the molding interface material is either polyimide or BCB.

4. (Previously Presented): A semiconductor package as recited in claim 1, wherein the molding interface material is on at least a portion of the plurality of side surfaces of the die.